Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1-6. (*canceled*)

7. (*currently amended*) An ESD protection circuit, comprising:

one or more first diodes ~~on a first area of P-substrate~~ coupled in series between a supply voltage and a terminal pad, each of said one or more first diodes having an n+ and a p+ diffusion region in an N-well on a first area of P-substrate;

a second diode ~~on said first area of P-substrate~~ coupled to a ground, said second diode having an n+ and a p+ diffusion region on said first area of P-substrate; and

one or more third diodes ~~on a second area of P-substrate~~ coupled in series between said terminal pad and said second diode, each of said one or more third diodes having an n+ and a p+ diffusion region on ~~said~~ a second area of P-substrate separated by a deep N-well from said first area of P-substrate.

8-9. (*canceled*)

10. (*previously presented*) The ESD protection circuit of claim 7, wherein said first area of P-substrate is coupled to said ground.

11. (*previously presented*) The ESD protection circuit of claim 7, wherein an allowable signal swing at said terminal pad is greater than said supply voltage plus 1.4 V.

12. (*previously presented*) The ESD protection circuit of claim 7, wherein a forward turn-on voltage of each of said one or more first diodes, said second diode, and said one or more third diodes is approximately 0.7 V.

13. (*currently amended*) An ESD protection circuit, comprising:

a first diode in a first N-well on a first area of P-substrate, said first diode having a cathode coupled to a supply voltage ~~and an anode coupled to a cathode of~~;

a second diode~~, said second diode~~ in a second N-well on said first area of P-substrate, said second diode having a cathode coupled to an anode of said first diode and an anode coupled to a terminal pad; ~~and~~

a third diode on a second area of P-substrate separated by a deep N-well from said first area of P-substrate, said third diode having a cathode coupled to said terminal pad ~~and an anode coupled to a cathode of~~; and

a fourth diode~~, said fourth diode~~ on said first area of P-substrate, said fourth diode having a cathode coupled to an anode of said third diode and an anode coupled to a ground~~, wherein said third diode includes an n+ region on said second area of P-substrate separated by a deep N-well from said first area of P-substrate, and wherein said fourth diode includes an n+ region on said first area of P-substrate~~.

14. (*currently amended*) The ESD protection circuit of claim 13, wherein said first diode and said second diode each includes an n+ and a p+ diffusion region in [[an]] said first and second N-wells, respectively, on said first area of P-substrate.

15. (*previously presented*) The ESD protection circuit of claim 13, wherein an interconnection node between said third diode and said fourth diode is isolated from said ground.

16. (*previously presented*) The ESD protection circuit of claim 13, wherein said first area of P-substrate is coupled to said ground.

17. (*previously presented*) The ESD protection circuit of claim 13, wherein an allowable signal swing at said terminal pad is greater than said supply voltage plus 1.4 V.

18. (*previously presented*) The ESD protection circuit of claim 13, wherein a forward turn-on voltage of each of said first diode, said second diode, said third diode, and said fourth diode is approximately 0.7 V.

19. (*new*) The ESD protection circuit of claim 13, wherein said third diode includes an n+ and a p+ diffusion region in said deep N-well.

20. (*new*) The ESD protection circuit of claim 13, wherein said fourth diode includes an n+ and a p+ diffusion region on said first area of P-substrate.

21. (*new*) The ESD protection circuit of claim 13, further comprising a plurality of said third diode coupled in series between said second diode and said fourth diode.

22. (*new*) The ESD protection circuit of claim 7, wherein an interconnection node between one of said third diodes and said second diode is isolated from said ground.